REMARKS/ARGUMENTS

Favorable reconsideration of this application, in light of the following discussion, is respectfully requested.

Claims 1-20 are pending in the present application.

In the outstanding Office Action, Claims 1, 4, 7-10, 12, 16, 17, and 20 were rejected under 35 U.S.C. § 103(a) as unpatentable over Nagao (U.S. Pat. No. 6,677,674) in view of Kimura et al. (U.S. Pat. No. 6,078,096, hereafter Kimura) and further in view of Kim et al. (U.S. Pat. No. 6,594,818, hereafter Kim); Claims 5, 6, 13-15, 18, and 19 were rejected under 35 U.S.C. § 103(a) as unpatentable over Nagao in view of Kimura and further in view of Kim and Majima (U.S. Pat. No. 4,408,875); and Claims 3 and 11 were objected to for depending from a rejected base claim, but were otherwise indicated as including allowable subject matter.

Applicant acknowledges with appreciation the indication that Claims 3 and 11 contain allowable subject matter. However, these claims have been presently maintained in dependent form because Applicant considers the pending independent claims patentably distinguishing over the applied art.

With regard to the outstanding rejection of Claims 1, 4, 7-10, 12, 16, and 17 under 35 U.S.C. § 103(a) as unpatentable over Nagao, that rejection is respectfully traversed.

Claim 1 relates to a COC device, comprising:

> a memory chip mounted on the logic chip, the memory chip comprising:
>
> basic chips functioning as a chip independently from each other; and
>
> a dicing line interposed between the basic chips, connecting the basic chips, and configuring a part of the memory chip....

Independent Claim 9 recites analogous features.

Through the claimed configuration, the memory capacitance of memory chips cut from one wafer may be freely varied depending on how the memory chips are cut. According to the claimed configuration, the dicing line is formed between basic chips to configure a part of the memory chips, and the dicing line does not have a logic circuit linking the basic chips therein. Accordingly, the way in which the memory chip is cut is not limited.

In response to the arguments submitted by Applicant on October 27, 2005, the outstanding Office Action, at page 8, states "As for claiming dicing line is missing from Kimura's patent is unacceptable because dicing and lining are mutually inclusive. The claim language concerning 'dicing line' is fully met by Kimura." Applicants respectfully traverse this position.

Furthermore, Applicants respectfully submit an excerpt from *Microchip Fabrication*, by Peter Van Zant (hereinafter Van Zant), to support their position.

The outstanding Office Action relies upon a combination of Nagao, Kimura, and Kim to anticipate the features of independent Claims 1 and 9. In more detail, the outstanding Office Action alleges that Kimura teaches that chips are separated from a mother wafer by dicing means.[1] In fact, Kimura does not disclose or suggest a dicing line, as recited in Claim 1. The term "dicing line" is a technically established term, which is distinct from the interconnection area of Kimura.

As evidenced by page 561 from Van Zant, a dicing line (or scribe line) is a line along which a wafer is cut in order to separate a basic chip from the wafer. An exemplary scribe line is shown in Fig. 18.15 of Van Zant (also on page 561).

As shown in Fig. 3 of Kimura, the four 4 Mbit DRAM 6 are not separated by a dicing line. On the contrary, the 4 Mbit DRAM 6 are connected to each through interconnection/controller circuits 7. A COC that includes the four 4 Mbit DRAM, as shown

[1] Applicants note that no specific passages of Kimura were cited to support this assertion.

in Fig. 3 of Kimura, does not disclose or suggest the claimed "dicing line interposed between the basic chips, connecting the basic chips, and configuring a part of the memory chip."

The Abstract of Kimura discloses that the interconnection controller circuit 7 is formed in the dicing area. However, the interconnection controller circuit 7 effectively replaces the dicing area. Thus, when a COC is formed using the four 4 Mbit DRAM shown in Fig. 3 of Kimura, the device does not equate to the claimed "...the memory chip comprising:...a dicing line interposed between the basic chips, connecting the basic chips, and configuring a part of the memory chip."

Furthermore, Kimura discloses a redundancy technology in which only one type of memory chip is cut from a wafer. For example, according to Figure 2 of Kimura, the area where the wafer is cut out is predetermined, and the memory chip is cut out in only one way. In the example in Figure 2 of Kimura, only a 16 Mbit memory chip (four 4 Mbit memory chips) may be cut from one wafer. Likewise, according to Figure 8 of Kimura, only an 8 Mbit memory chip (two 4 Mbit memory chips) can be cut from a wafer. As further illustrated in Figures 5-7 of Kimura, when a faulty area is discovered, the faulty area is not treated as a defective chip. Rather, the faulty area is discarded by dicing.[2]

In Kimura, a logic circuit 7 linking basic chips is provided between the basic chips to perform redundancy. For example, as shown in Figure 9 of Kimura, logic circuit 7 transmits and receives signals between two basic chips. In this case, the area between the basic chips (e.g., dicing line 5_5, 5_6) is used to discard the faulty area from the chips.

By contrast, the dicing line of the present invention excludes a logic circuit linking the basic chips. In fact, according to the claimed invention, the basic chips divided by the dicing line must be mutually independent. As a result, it is respectfully submitted that Kimura does not disclose or suggest the dicing line of Claim 1.

[2] Kimura, col. 4, lines 62 - col. 5, line 7.

Moreover, because the basic chips of Kimura are always interdependent, it is not possible to combine the teachings of Kimura with Kim. Kim describes mutually exclusive chips.[3] Therefore, to combine the teachings of Kimura, which relates to interdependent chips with the disclosure of Kim, which relates to exclusive chips, is contrary to the teachings of each of these references.

As set forth in MPEP § 2143.01, the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680 (Fed. Cir. 1990). Furthermore, the proposed modification cannot change the principle of operation of a reference. In other words, if the proposed modification or combination of the prior art would change the principle of operation the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. In re Ratti, 270 F.2d 810 (CCPA 1959).

In this case, because the outstanding Office Action proposes to modify the teachings of a reference (Kimura) which describes interdependent chips with the teachings of another reference (Kim) which teaches mutually exclusive chips, it is respectfully submitted that the outstanding Office Action has violated the requirements set forth in MPEP § 2143.01. In more detail, changing the interdependent chips of Kimura to include mutually exclusive chips changes Kimura's principle of operation.

Therefore, the outstanding Office Action has violated the requirements of MPEP § 2143.01, and it is respectfully submitted that the outstanding Office Action has failed to provide a *prima facie* case of obviousness with respect to Claims 1, 4, 7-10, 12, 16, and 17.

Because the outstanding Office Action has not provided a *prima facie* case of obviousness, it is respectfully requested that this rejection be withdrawn.

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[3] See, Kim, Abstract.

Likewise, the rejection of Claims 5, 6, and 13-15 is also respectfully traversed. Claims 5 and 6 depend from Claim 1, and Claims 13-15 depend from Claim 9. As noted above, the combination of Nagao, Kimura, and Kim does not provide a *prima facie* case of obviousness with respect to the features of Claims 1 and 9. Because Majima is not relied upon to provide the features identified as deficient in the applied combination, Majima is not substantively addressed herewith.

Therefore, as the outstanding Office Action has not provided a *prima facie* case of obviousness with respect to Claims 5, 6, and 13-15, it is respectfully requested that this rejection be withdrawn.

Consequently, in view of the foregoing discussion, it is respectfully submitted that this application is in condition for allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,

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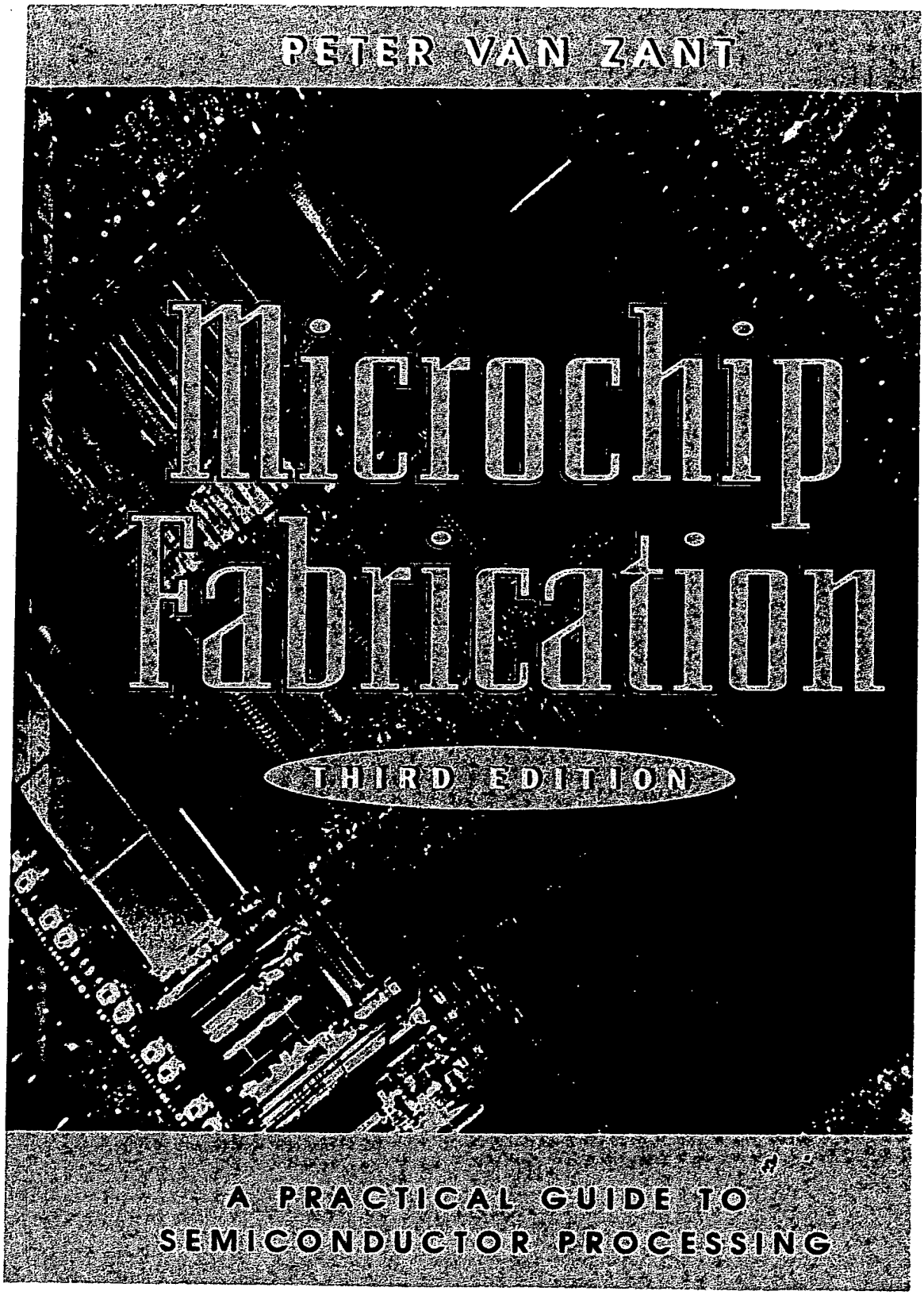

Microchip Fabrication

A Practical Guide to Semiconductor Processing

Peter Van Zant

Third Edition

McGraw-Hill

New York San Francisco Washington, D.C. Auckland Bogotá
Caracas Lisbon London Madrid Mexico City Milan
Montreal New Delhi San Juan Singapore
Sydney Tokyo Toronto

Library of Congress Cataloging-in-Publication Data

Van Zant, Peter.
Microchip fabrication : a practical guide to semiconductor processing / Peter Van Zant.—3rd ed.
p. cm.
Includes index.
ISBN 0-07-067250-4 (hardcover)
1. Semiconductors—Design and construction. I. Title.
IN PROCESS
621.3815'2—dc20 96-15729
CIP

McGraw-Hill

A Division of The McGraw-Hill Companies

1 2 3 4 5 6 7 8 9 0 DOC/DOC 9 0 1 0 9 8 7 6

ISBN 0-07-067250-4

The sponsoring editor for this book was Steve Chapman, the editing supervisor was Fred Bernardi, and the production supervisor was Pamela Pelton. It was set in Century Schoolbook by Dina E. John of McGraw-Hill's Professional Book Group composition unit.

Printed and bound by R. R. Donnelley & Sons Company.

This book is printed on recycled, acid-free paper containing a minimum of 50% recycled, de-inked fiber.

When ordering this title, use ISBN 0-07-114837-X.

to the wafer diameter. Stresses induced in the wafer by the grinding and polishing processes must be controlled to prevent wafer and die warping. Wafer warping interferes with the die separation process (broken and cracked die). Die warping creates die-attach problems in the packaging process.[2]

Backside gold. Another optional wafer process is adding a layer of backside gold. A layer of gold is required on wafers that are going to be attached to the package by eutectic techniques (see the "Die attach" section). The gold is usually applied in the fabrication area (after backgrinding) by evaporation or sputtering.

Die separation

The chip-packaging process starts with the separation of the wafer into individual dies. The two methods of die separation are scribing and sawing (Fig. 18.15).

Scribing. *Scribing,* or *diamond scribing,* was the first production die-separation technique developed in the industry. It requires the alignment of the wafer on a precision stage, followed by dragging a diamond-tipped scribe through the center of the scribe lines. The scribe creates a shallow scratch in the wafer surface. The separation of the die is completed by stressing the wafer with a cylindrical roller. As the roller is moved over the surface, the wafer separates along the scribe lines. The breaks follow the crystal structure of the wafer, thus creating a right-angle edge on the die. Scribing becomes unreliable in wafers over 10 mils thick.

Sawing. The advent of thicker wafers has led to the development of sawing as the preferred die-separation method. A saw consists of a wafer table with rotation capability, a manual or automatic vision system for orienting the scribe lines, and a diamond-impregnated round saw. Two techniques are used. Both start with the passage of

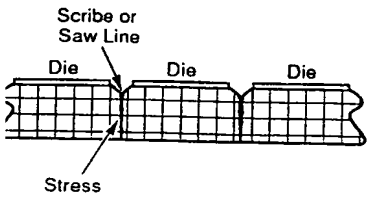

Figure 18.15 Scribe and saw separation.